UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Offic
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Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/537,274	03/29/00	MOSLEY	L 884.240US1

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EXAMINER	
THOMAS, E	
ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 05/23/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/537,274	MOSLEY, LARRY EUGENE	
	Examiner	Art Unit	
	Eric W Thomas	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2000* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 200, 420. Correction is required.

The drawings are objected to because

"410" has been designated "vias" not "a capacitor" (not pointing to the vias).

Correction is required.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "440" has been used to designate both vias and conductive layer. Correction is required.

Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6, 14-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "the plurality of plurality" in line 3 (& 5). There is insufficient antecedent basis for this limitation in the claim. It examiner interpreted this limitation as "the circuit package".

Claim 14 recites the limitation "the circuit board " in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claims 15-18, line 1, change "the circuit board" to –The circuit package--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 14-16, & 19, are rejected under 35 U.S.C. 102(e) as being anticipated by Farooq et al. (US 6,072,690).

Regarding claim 1, Farooq et al. disclose in fig. 3C, a multilayer integrated circuit capacitor comprising: a substrate (72); a first conductive layer (68) located over the substrate; a first insulator layer (72) located over the first conductive layer; a second conductive layer (67) located over the first insulator layer; a second insulator layer (72) located over the second conductive layer; a third conductive layer (68) located over the second insulator layer; a third insulator layer (72) located over the third conductor layer;

and a plurality of conductive vias (64, 66) downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductor layers.

Regarding claim 2, Farooq et al. further comprises a plurality of controlled collapse chip connection (C4) lands fabricated on the third insulator layer and in electrical contact with the plurality of conductive vias (col. 3 lines 25-30).

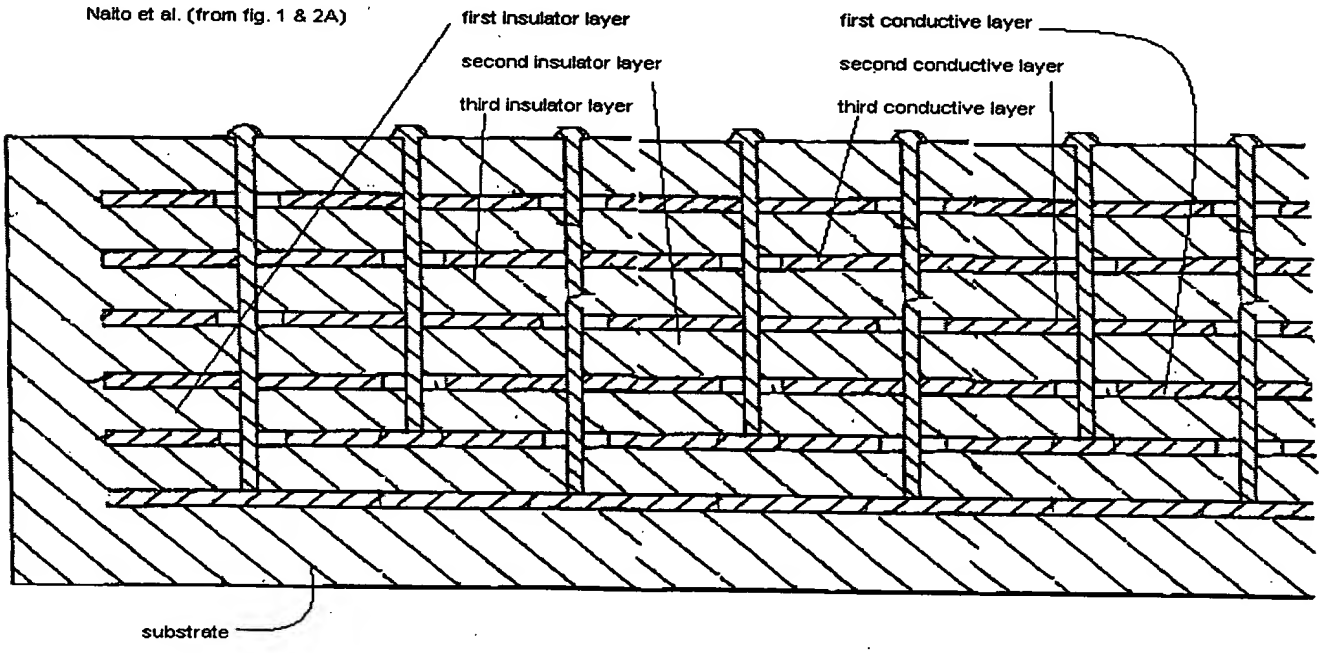
Regarding claim 14, Farooq et al. disclose in fig. 1, & 3C, a package having supply voltage interconnect (col. 3 lines 3-12) lines; a first integrated circuit die mounted on a circuit package (see fig. 1) a second integrated die mounted on the circuit and electrically connected to the supply voltage interconnect lines, the second integrated circuit package comprises a capacitor comprising: a substrate (72); a first conductive layer (68) located over the substrate; a first insulator layer (72) located over the first conductive layer; a second conductive layer (67) located over the first insulator layer; a second insulator layer (72) located over the second conductive layer; a third conductive layer (68) located over the second insulator layer; a third insulator layer (72) located over the third conductor layer; and a plurality of conductive vias (64, 66) downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductor layers.

Regarding claim 15, Farooq et al. further comprises a plurality of controlled collapse chip connection (C4) lands fabricated on the third insulator layer and in electrical contact with the plurality of conductive vias (col. 3 lines 25-30).

Regarding claim 16, Farooq disclose the first integrated circuit package is a processor (see col. 1 lines 11-45).

Regarding claim 19, Farooq et al. disclose in fig. 3C, a multi layer integrated circuit capacitor comprising: a substrate (72); a first conductive layer (68) located over the substrate; a first insulator layer (72) located over the first conductive layer; a second conductive layer (67) located over the first insulator layer; a second insulator layer (72) located over the second conductive layer; a third conductive layer (68) located over the second insulator layer; a third insulator layer (72) located over the third conductive layer; and a plurality of conductive vias (64, 66) downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductive layers, the plurality of conductive vias further extend through the substrate to provide electrical interconnects on both a top and a bottom surface of the integrated circuit capacitor.

Claims 1, 8, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Naito et al. (EP 0, 917,165 A2).



Naito et al. disclose in fig. 1 & 2, a multilayer integrated circuit capacitor comprising: a substrate; a first conductive layer (33) located over the substrate; a first insulator layer (32) located over the first conductive layer; a second conductive layer (34) located over the first insulator layer; a second insulator layer (32) located over the second conductive layer; a third conductive layer (33) located over the second insulator layer; a third insulator layer (32) located over the third conductor layer; and a plurality of conductive vias (40,41) downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductor layers.

Regarding claim 8, some of the plurality of conductive vias (40) pass through the second conductive layer without forming an electrical connection with the second conductive layer.

Regarding claim 11, Naito et al. disclose in fig. 1 & 2, a multi layer integrated circuit capacitor comprising: a substrate; a first conductive layer (34)located over the substrate; a first insulator layer (32) located over the first conductive layer; a second conductive layer (33) located over the first insulator layer; a second insulator layer (32) located over the second conductive layer; a third conductive layer (34) located over the second insulator layer; a third insulator layer (32) located over the third conductive layer; a first plurality of conductive vias (41) downwardly extending through the third insulator layer, third conductive layer, second insulator layer, second conductive layer and the first insulator layer to provide electrical interconnect to the first and third conductive layers; and a second plurality of conductive vias (40) downwardly extending

through the third insulator layer, third conductive layer and second insulator layer to provide electrical interconnect to the second conductive layer.

Claims 1, 7, & 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Watt (US 5,745,335).

Regarding claim 1, Watt discloses in fig. 1, a multilayer integrated circuit capacitor comprising: a substrate (1, 2); a first conductive layer (7) located over the substrate; a first insulator layer (22b) located over the first conductive layer; a second conductive layer (8) located over the first insulator layer; a second insulator layer (24b) located over the second conductive layer; a third conductive layer (9) located over the second insulator layer; a third insulator layer (10) located over the third conductor layer; and a plurality of conductive vias (40, 38, 46) downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductor layers.

Regarding claim 7, the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer.

Regarding claim 9, Watt discloses in fig. 1 (5-6 – fig. 5 & 6 illustrates two conductor layers), a multilayer integrated circuit capacitor comprising: a substrate (1, 2); a first conductive layer (7) located over the substrate; a first insulator layer (22b) located over the first conductive layer; a second conductive layer (8) located over the first insulator layer; (as seen in fig. 5-6) the second conductive layer is fabricated as a

plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer; a second insulator layer (24b) located over the second conductive layer; a third conductive layer (9) located over the second insulator layer; the third conductive layer is fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer; a third insulator layer (10) located over the third conductor layer; and a first plurality of conductive vias (40 + as seen in the 3rd drawing of fig. 5) downwardly extending through the third insulator layer to provide electrical interconnect to the third conductor layers; a second plurality of conductive vias (38 + as seen in the 3rd drawing of fig. 5) downwardly extending through the third insulator layer to provide electrical interconnect to second conductor layer; a third plurality of conductive vias (46 + as seen in the 3rd drawing of fig. 5) downwardly extending through the third insulator layer to provide electrical interconnect to the first conductor layers.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naito et al. (EP 0, 917,165 A2) in view of Farooq et al. (US 6,072,690).

Regarding claim 2, Naito et al. disclose the claimed invention except for the C4 lands in electrical contact with the plurality of vias. Farooq et al. teach the use of C4 lands in multilayer integrated circuit capacitors. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form C4 lands on the capacitor of Naito et al. (in which the C4 lands electrically connect the plurality of vias), since such a modification (is well known in the art) would improve the external connections to electrical components.

Regarding claim 3, Naito et al. disclose in fig. 2, the C4 lands are fabricated in staggered columns in a plan view.

Claims 4-5, 13, & 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naito et al. (EP 0, 917,165 A2)

Regarding claim 4 (& 21), Naito et al. disclose the claimed invention except for the insulators are fabricated by a BaSrTiO3 material. BaSrTiO3 is a well known dielectric (insulator) used in the capacitor art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the insulators of Naito et al. using BaSrTiO3, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 5, Naito et al. disclose the claimed invention except for the metal conductors are fabricated from a copper material. Copper is a well known

material used as conductors in the capacitor art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductors of Naito et al. using a copper material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 13, Naito et al. disclose the claimed invention except for the insulators are fabricated by a BaSrTiO3 material. BaSrTiO3 is a well known dielectric (insulator) used in the capacitor art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the insulators of Naito et al. using BaSrTiO3, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Claims 6, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt (US 5,745,335) in view of Yach et al. (US 6,225,678).

Watt discloses the claimed invention, except for the fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnected lines the selectively connect the plurality of conductive vias. Yach et al. teach a plurality of capacitors can be connected through a interconnect line. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of Watt capacitors; since such a modification would connect a plurality of like capacitors together providing a particular capacitance for a system.

Regarding claim 10, Watt discloses the claimed invention except for a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnected lines the selectively connect the plurality of conductive vias. Yach et al. teach a plurality of capacitors can be connected through a interconnect line. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of Watt capacitors; since such a modification would connect a plurality of like capacitors together providing a particular capacitance for a system.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naito et al. (EP 0, 917,165 A2) in view of Yach et al. (US 6,225,678).

Naito et al. disclose the claimed invention except for a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnected lines the selectively connect the plurality of conductive vias. Yach et al. teach a plurality of capacitors can be connected through a interconnect line. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of Naito et al. capacitors; since such a modification would connect a plurality of like capacitors together providing a particular capacitance for a system.

Claims 18, & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq et al in view of Yach et al. (US 6,225,678).

Regarding claims 18, & 20, Farooq et al. disclose the claimed invention except for a fourth conductive layer located over the third insulator layer, the fourth conductive

layer is patterned to form interconnected lines the selectively connect the plurality of conductive vias. Yach et al. teach a plurality of capacitors can be connected through a interconnect line. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of Farooq et al. capacitors; since such a modification would connect a plurality of like capacitors together providing a particular capacitance for an electrical system.

Claims 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq et al.

Farooq et al. disclose the claimed invention except for the insulators are fabricated by a BaSrTiO3 material. BaSrTiO3 is a well known dielectric (insulator) used in the capacitor art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the insulators of Farooq et al. using BaSrTiO3, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Double Patenting

Applicant is advised that should claim 4 be found allowable, claim 21 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is (703) 305-0878. The examiner can normally be reached on Mon-Thur & alternating Friday 6:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 703-308-3682. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-7722 for regular communications and (703) 305-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 357-5076.

ewt
May 19, 2001

Dean A. Reichard 5/21/01
Dean A. Reichard
Primary Examiner